REMARKS

Claims 1-19 are presented for examination. Claim 8 is found allowable subject to being rewritten in independent form.

Claims 1-4, 7- 9-15, 17 and 19 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kuroda. Dependent claims 5, 6, 16 and 18 have been rejected under 35 U.S.C. § 103 as being unpatentable over Kuroda in view of Bowen et al.

To more clearly define the claimed invention, claims 1 and 12 have been amended. Claim 1 recites

Claim 1, as amended, recites a memory system for a portable telephone including a signal transmission/reception portion for transmitting and receiving a signal and a control portion for controlling at least a signal transmission and reception operation of said transmission/reception portion. The memory system comprises:

- a random access memory providing a working area for said control portion; and

- a flash memory including a memory array for storing a program for said control portion and at least transmission and reception data in a non-volatile manner under a control of said control portion.

Claim 1 specifies that the memory array is divided into a plurality of storage units, and a register, provided commonly to the respective storage units, and having information in a storage unit of said plurality of storage units transmitted thereinto for temporal storage of the transmitted information and allowing serial readout of the transmitted and stored information.

As demonstrated below, Kuroda neither teach nor suggests the claimed register provided commonly to the respective storage units and having information in a storage unit of said plurality

of storage units transmitted thereinto for temporal storage of the transmitted information and allowing serial readout of the transmitted and stored information.

The Examiner considers the memory sections ARY0-ARY7 (FIGS. 13 and 35 of Kuroda) to correspond to the plurality of storage units. The data line CD is considered to correspond to the claimed register. The Examiner takes the position that the data line CD allows information in each memory section to be read out serially in synchronization with a clock signal. The Examiner relies upon the disclosure in col. 14, line 50 to col. 15, line 4 and in col. 24, line 6-14.

Considering these portions of the specification, Kuroda discloses that the data lines in each of the memory sections ARY0-ARY7 are connected to a common data line CD. The data from each memory cell MC are read out to the data line CD.

However, the data line CD is not a register. Moreover, the reference does not disclose that information in a storage unit of the plurality of storage units is transmitted into the data line CD for temporal storage of the transmitted information, and that the data line CD allows serial readout of the transmitted and stored information, as claim 1, as amended, requires.

Moreover, Kuroda does not disclose that the data line CD is common to respective memory sections, as claim 1 requires. Instead, the reference discloses that each memory section has its own data line CD independent of data lines CD in the other memory sections.

Accordingly, Kuroda does not teach or suggest the subject matter of claim 1.

Further, independent claim 12 also recites that the memory array is divided into a plurality of storage units. The claim, as amended, specifies that a plurality of pieces of information in one unit of the storage units selected in accordance with an address signal at a time, are allowed to be serially read out in synchronization with a clock signal without further address application, i.e. the

serial data transmission is performed in synchronization with the clock signal in response to one-time application of an address signal without further address application.

The Examiner relies upon FIG. 28 of Kuroda for disclosing the serial readout in synchronization with a clock signal. However, as shown in FIG. 28, an address signal PAS is applied in synchronization with the clock signal. Memory selection is designated by memory delection instruction MS-FLN. Data output is designated in accordance with output enable M2RDN, and data read out by sense amplifier is latched into the latch circuit and then externally output.

Hence, memory cell selection of Kuroda is carried out in accordance with an address signal and data the selected memory cell is read out in data reading. The clock cycle is defined by the clock signal which does not provide the data output timing from the latch.

Accordingly, Kuroda does not teach or suggest that a plurality of pieces of information in one unit of the storage units selected in accordance with an address signal at a time, are allowed to be serially read out in synchronization with a clock signal without further address application, as amended claim 12 requires.

Dependent claim 2-7, 9-11, and 13-19 are defined over the prior art at least for the reasons presented above in connection with claims 1 and 12.

In view of the foregoing, and in summary, claims 1-19 are considered to be in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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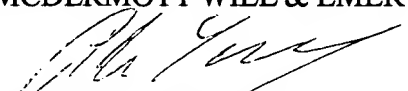

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